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IEEE JNL	IEEE Journal or Magazine
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IEEE CNF	IEEE Conference Proceeding
IEE CNF	IEE Conference Proceeding
IEEE STD	IEEE Standard

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1. **A model for transient fault propagation in combinatorial logic**
Oman, M.; Papasso, G.; Rossi, D.; Metra, C.;
On-Line Testing Symposium, 2003. IOLTS 2003. 9th IEEE
7-9 July 2003 Page(s):111 - 115
Digital Object Identifier 10.1109/OLT.2003.1214376
AbstractPlus | Full Text: PDF(389 KB) IEEE CNF

2. **Margins and yield in single flux quantum logic**
Hamilton, C.A.; Gilbert, K.C.;
Applied Superconductivity, IEEE Transactions on
Volume 1, Issue 4, Dec. 1991 Page(s):157 - 163
Digital Object Identifier 10.1109/77.107400
AbstractPlus | Full Text: PDF(540 KB) IEEE JNL

3. **Proceedings. The European Conference on Design Automation (Cat. No.92TH0414-3)**
Design Automation, 1992. Proceedings. [3rd] European Conference on
16-19 March 1992
Digital Object Identifier 10.1109/EDAC.1992.205874
AbstractPlus | Full Text: PDF(16 KB) IEEE CNF

4. **Network Partitioning and Ordering for MOS VLSI Circuits**
Rao, V.B.; Trick, T.N.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on
Volume 6, Issue 1, January 1987 Page(s):128 - 144
AbstractPlus | Full Text: PDF(2560 KB) IEEE JNL

5. **Estimation of sequential circuit activity considering spatial and temporal correlations**
Tan-Li Chou; Roy, K.;
Computer Design: VLSI in Computers and Processors, 1995. ICCD '95. Proceedings., 1995 IEEE International Conference on
2-4 Oct. 1995 Page(s):577 - 582
Digital Object Identifier 10.1109/ICCD.1995.528926
AbstractPlus | Full Text: PDF(528 KB) IEEE CNF

6. **Hierarchical topological sorting of apparent loops via partitioning**
Beetem, J.F.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on

Volume 11, Issue 5, May 1992 Page(s):607 - 619
Digital Object Identifier 10.1109/43.127622

AbstractPlus | Full Text: PDF(872 KB) IEEE JNL

7. **Monte Carlo optimization of superconducting complementary output switching logic circuits**
Jeffery, M.; Perold, W.J.; Zuoqin Wang; van Duzer, T.;
Applied Superconductivity, IEEE Transactions on
Volume 8, Issue 3, Sept. 1998 Page(s):104 - 119
Digital Object Identifier 10.1109/77.712141

AbstractPlus | References | Full Text: PDF(484 KB) IEEE JNL

8. **Complementary output switching logic-a new superconducting voltage-state logic family**
Perold, W.J.; Jeffery, M.; Zuoqin Wang; Van Duzer, T.;
Applied Superconductivity, IEEE Transactions on
Volume 6, Issue 3, Sept. 1996 Page(s):125 - 131
Digital Object Identifier 10.1109/77.544779

AbstractPlus | References | Full Text: PDF(904 KB) IEEE JNL

9. **New multi-flux-quantum logic family**
Kaphmenko, V.K.; Wikborg, E.;
Applied Superconductivity, IEEE Transactions on
Volume 7, Issue 2, Part 3, June 1997 Page(s):2288 - 2291
Digital Object Identifier 10.1109/77.621695

AbstractPlus | References | Full Text: PDF(456 KB) IEEE JNL

10. **Identification and classification of single-event upsets in the configuration memory of SRAM-based FPGAs**
Ceschia, M.; Violante, M.; Reorda, M.S.; Paccagnella, A.; Bernardi, P.; Rebaudengo, M.; Bortolato, D.; Bellato, M.; Zambolin, P.; Candelori, A.;
Nuclear Science, IEEE Transactions on
Volume 50, Issue 6, Part 1, Dec. 2003 Page(s):2088 - 2094
Digital Object Identifier 10.1109/TNS.2003.821411

AbstractPlus | References | Full Text: PDF(315 KB) IEEE JNL

11. **Proceedings of 1993 IEEE International Conference on Computer Design ICCD'93**
Computer Design: VLSI in Computers and Processors, 1993. ICCD '93. Proceedings., 1993 IEEE International Conference on
3-6 Oct. 1993
Digital Object Identifier 10.1109/ICCD.1993.393415

AbstractPlus | Full Text: PDF(20 KB) IEEE CNF

12. **Planar approximation for the least reliable bit log-likelihood ratio of 8-PSK modulation**
Thesling, W.H.; Xiong, F.; Vanderaar, M.J.;
Communications, IEE Proceedings-
Volume 147, Issue 3, June 2000 Page(s):144 - 148
Digital Object Identifier 10.1049/ip-com:20000178

AbstractPlus | Full Text: PDF(344 KB) IEE JNL

13. **A family of CMOS latches with 3 stable operating points**
Xiaoqiang Shou; Green, M.M.;
Circuits and Systems, 2001. ISCAS 2001. The 2001 IEEE International Symposium on
Volume 1, 6-9 May 2001 Page(s):109 - 112 vol. 1
Digital Object Identifier 10.1109/ISCAS.2001.921800

AbstractPlus | Full Text: PDF(228 KB) IEEE CNF

14. **Design diversity for concurrent error detection in sequential logic circuits**
Mitra, S.; McCluskey, E.J.;

VLSI Test Symposium, 19th IEEE Proceedings on. VTS 2001
29 April-3 May 2001 Page(s):178 - 183
Digital Object Identifier 10.1109/VTS.2001.923436

AbstractPlus | Full Text: PDF(532 KB) IEEE CNF

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((((simulat* and (combinatorial logic or state logic))<in>metadata))<and>((simulat* an

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» Key

IEEE JNL	IEEE Journal or Magazine
IEE JNL	IEE Journal or Magazine
IEEE CNF	IEEE Conference Proceeding
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IEEE STD	IEEE Standard

Select Article Information

1. **Monte Carlo optimization of superconducting complementary output switching logic circuits**
Jeffery, M.; Perold, W.J.; Zuoqin Wang; van Duzer, T.;
Applied Superconductivity, IEEE Transactions on
Volume 8, Issue 3, Sept. 1998 Page(s):104 - 119
Digital Object Identifier 10.1109/77.712141
AbstractPlus | References | Full Text: PDF(484 KB) IEEE JNL

2. **Design diversity for concurrent error detection in sequential logic circuits**
Mitra, S.; McCluskey, E.J.;
VLSI Test Symposium, 19th IEEE Proceedings on. VTS 2001
29 April-3 May 2001 Page(s):178 - 183
Digital Object Identifier 10.1109/VTS.2001.923436
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Terms used **simulation** and **logic design** and **combinatorial logic** and **state logic** and **graphic elementS**

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1 A functional level simulation engine of MAN-YO: a special purpose parallel machine for logic design automation

T. Nakata, N. Koike

June 1986 **ACM SIGARCH Computer Architecture News , Proceedings of the 13th annual international symposium on Computer architecture**, Volume 14 Issue 2

Full text available: pdf(511.58 KB) Additional Information: full citation, abstract, references, index terms

The architecture of a proto-type functional level simulator element of a massively parallel machine (MAN-YO) designed for logic design automation is presented. At functional level, hardware systems are described in a hardware description language, FDL. The FDL description is compiled into stack oriented intermediate language instructions. Communicating with other gate level/block level/ functional level processors, each functional simulator interprets the compiled instructions and simulates ...

2 Curriculum 68: Recommendations for academic programs in computer science: a report of the ACM curriculum committee on computer science

William F. Atchison, Samuel D. Conte, John W. Hamblen, Thomas E. Hull, Thomas A. Keenan, William B. Kehl, Edward J. McCluskey, Silvio O. Navarro, Werner C. Rheinboldt, Earl J. Schweppe, William Viavant, David M. Young

March 1968 **Communications of the ACM**, Volume 11 Issue 3

Full text available: pdf(6.63 MB) Additional Information: full citation, references, citings

Keywords: computer science academic programs, computer science bibliographies, computer science courses, computer science curriculum, computer science education, computer science graduate programs, computer science undergraduate programs

3 Combinational logic synthesis for LUT based field programmable gate arrays

Jason Cong, Yuzheng Ding

April 1996 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 1 Issue 2

Full text available: pdf(628.91 KB) Additional Information: full citation, abstract, references, citings, index terms, review

The increasing popularity of the field programmable gate-array (FPGA) technology has generated a great deal of interest in the algorithmic study and tool development for FPGA-

specific design automation problems. The most widely used FPGAs are LUT based FPGAs, in which the basic logic element is a K-input one-output lookup-table (LUT) that can implement any Boolean function of up to K variables. This unique feature of the LUT has brought new challenges to lo ...

Keywords: FPGA, area minimization, computer-aided design of VLSI, decomposition, delay minimization, delay modeling, logic optimization, power minimization, programmable logic, routing, simplification, synthesis, system design, technology mapping

4 Logic verification methodology for PowerPC microprocessors

Charles H. Malley, Max Dieudonné

January 1995 **Proceedings of the 32nd ACM/IEEE conference on Design automation**

Full text available: pdf(69.13 KB) Additional Information: full citation, references, citings, index terms

5 Computing curricula 2001

September 2001 **Journal on Educational Resources in Computing (JERIC)**

Full text available: pdf(613.63 KB) html(2.78 KB) Additional Information: full citation, references, citings, index terms

6 Parallel logic programming systems

Jacques Chassin de Kergommeaux, Philippe Codognet

September 1994 **ACM Computing Surveys (CSUR)**, Volume 26 Issue 3

Full text available: pdf(3.51 MB) Additional Information: full citation, abstract, references, citings, index terms

Parallelizing logic programming has attracted much interest in the research community, because of the intrinsic OR- and AND-parallelisms of logic programs. One research stream aims at transparent exploitation of parallelism in existing logic programming languages such as Prolog, while the family of concurrent logic languages develops language constructs allowing programmers to express the concurrency—that is, the communication and synchronization between parallel processes—withi ...

Keywords: AND-parallelism, OR-parallelism, Prolog, Warren Abstract Machine, binding arrays, concurrent constraint programming, constraints, guard, hash windows, load balancing, massive parallelism, memory management, multisequential implementation techniques, nondeterminism, scheduling parallel tasks, static analysis

7 Special issue on knowledge representation

Ronald J. Brachman, Brian C. Smith

February 1980 **ACM SIGART Bulletin**, Issue 70

Full text available: pdf(13.13 MB) Additional Information: full citation, abstract

In the fall of 1978 we decided to produce a special issue of the SIGART Newsletter devoted to a survey of current knowledge representation research. We felt that there were twe useful functions such an issue could serve. First, we hoped to elicit a clear picture of how people working in this subdiscipline understand knowledge representation research, to illuminate the issues on which current research is focused, and to catalogue what approaches and techniques are currently being developed. Secon ...

8 The FINITE STRING Newsletter: Abstracts of current literature

Computational Linguistics Staff
January 1987 **Computational Linguistics**, Volume 13 Issue 1-2

Full text available: pdf(6.15 MB) Additional Information: full citation
Publisher Site

9 An FPGA-based digital logic lab for computer organization and architecture
Mark Hoffman
May 2004 **Journal of Computing Sciences in Colleges**, Volume 19 Issue 5

Full text available: pdf(189.97 KB) Additional Information: full citation, abstract, references

The number of core hours devoted to digital logic in the knowledge unit Computer Architecture (AR) has been significantly reduced with the publication of *Computing Curricula 2001* (CC2001). Over half of core hours removed come at the expense of digital logic and digital systems. We have argued elsewhere that more digital logic must be included in Computer Architecture. In this paper, we present our experience with an FPGA-based digital logic lab offered with our undergraduate Computer Orga ...

10 Technical reports
SIGACT News Staff
January 1980 **ACM SIGACT News**, Volume 12 Issue 1

Full text available: pdf(5.28 MB) Additional Information: full citation

11 Special section: Reasoning about structure, behavior and function
B. Chandrasekaran, Rob Milne
July 1985 **ACM SIGART Bulletin**, Issue 93

Full text available: pdf(5.13 MB) Additional Information: full citation, abstract, references

The last several years' of work in the area of knowledge-based systems has resulted in a deeper understanding of the potentials of the current generation of ideas, but more importantly, also about their limitations and the need for research both in a broader framework as well as in new directions. The following ideas seem to us to be worthy of note in this connection.

12 Annealing placement by thermodynamic combinatorial optimization
Juan D Vicente, Juan Lanchares, Román Hermida
July 2004 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 9 Issue 3

Full text available: pdf(211.83 KB) Additional Information: full citation, abstract, references, index terms

Placement is key issue of integrated circuit physical design. There exist some techniques inspired in thermodynamics coping with this problem as Simulated Annealing. In this article, we present a combinatorial optimization method directly derived from both Thermodynamics and Information Theory. In TCO (Thermodynamic Combinatorial Optimization), two kinds of processes are considered: microstate and macrostate transformations. Applying the Shannon's definition of entropy to reversible microstate t ...

Keywords: Recofigurable, combinatorial optimization, entropy, information theory, programmable logic, thermodynamics

13 A design flow for partially reconfigurable hardware
Ian Robertson, James Irvine

May 2004 **ACM Transactions on Embedded Computing Systems (TECS)**, Volume 3 Issue 2

Full text available: pdf(698.30 KB) Additional Information: full citation, abstract, references, index terms

This paper presents a top-down designer-driven design flow for creating hardware that exploits partial run-time reconfiguration. Computer-aided design (CAD) tools are presented, which complement conventional FPGA design environments to enable the specification, simulation (both functional and timing), synthesis, automatic placement and routing, partial configuration generation and control of partially reconfigurable designs. Collectively these tools constitute the dynamic circuit switching CAD f ...

Keywords: FPGA, Viterbi decoder, configuration control, dynamically reconfigurable logic (DRL), power estimation, run-time reconfiguration (RTR)

14 Strategic directions in constraint programming

Pascal Van Hentenryck, Vijay Saraswat

December 1996 **ACM Computing Surveys (CSUR)**, Volume 28 Issue 4

Full text available: pdf(402.08 KB) Additional Information: full citation, references, citings, index terms

15 Logic and logic programming

J. A. Robinson

March 1992 **Communications of the ACM**, Volume 35 Issue 3

Full text available: pdf(6.56 MB) Additional Information: full citation, references, citings, index terms

Keywords: unification

16 State of the art and trends in Design Automation in Italy.

P. Ciompi, L. Simoncini, M. Tomljanovich, G. Valle

January 1975 **Proceedings of the 12th conference on Design automation**

Full text available: pdf(544.78 KB) Additional Information: full citation, abstract, references, index terms

A paper, which wants to deal, in the most comprehensive way, about the state of the art in Italy of Design Automation, that is a field which has a direct impact with the industrial reality of the country, presents some difficulty in the acquisition of the informations, which often are confidential or secret. Therefore most of the informations, on which this paper is based, are from the open literature, and therefore report the situation of one or two years ago.

17 The modular logic machine design system for loosely coupled systems

K. J. Burkhardt, J. J. DeSanto

January 1977 **Proceedings of the 1977 annual conference**

Full text available: pdf(630.53 KB) Additional Information: full citation, abstract, references, index terms

The recent introduction of complex integrated circuits in the form of microcomputers, microprocessors and single-chip arithmetic processors has put a new tool in the hands of the digital system designer. One area where these complex integrated circuits have not been fully utilized is in the design of high-performance computer systems. This lack of use can probably be attributed to the fact that the majority of existing high-performance systems have relied on rigid control mechanisms to obta ...

18 Performance and dependability evaluation of scalable massively parallel computer

systems with conjoint simulation
Axel Hein, Mario Dal Cin
October 1998 **ACM Transactions on Modeling and Computer Simulation (TOMACS)**, Volume 8 Issue 4

Full text available: pdf(501.59 KB) Additional Information: full citation, abstract, references, citings, index terms, review

Computer systems are becoming more and more a part of our daily life; business and industry rely on their service, and the health of human beings depends on their correct functioning. Computer systems used for critical tasks have to be carefully designed and tested during the early design stage, the prototype phase, and their operational life. Methods and tools are required to support and facilitate this vital task. In this article, we tackle the issue of system-level performance and depen ...

Keywords: fault-tolerant and large-scale computer systems, hierarchical model design, object-oriented modeling, process-based simulation, timed Petri nets

19 Composition and refinement of discrete real-time systems
Jonathan S. Ostroff
January 1999 **ACM Transactions on Software Engineering and Methodology (TOSEM)**, Volume 8 Issue 1

Full text available: pdf(1.59 MB) Additional Information: full citation, abstract, references, index terms, review

Reactive systems exhibit ongoing, possibly nonterminating, interaction with the environment. Real-time systems are reactive systems that must satisfy quantitative timing constraints. This paper presents a structured compositional design method for discrete real-time systems that can be used to combat the combinatorial explosion of states in the verification of large systems. A composition rule describes how the correctness of the system can be determined from the correctne ...

Keywords: abstraction, model-checking, modules, refinement, state explosion, temporal logic, timed logic

20 Constraint logic programming languages
Jacques Cohen
July 1990 **Communications of the ACM**, Volume 33 Issue 7

Full text available: pdf(3.85 MB) Additional Information: full citation, abstract, references, citings, index terms, review

Constraint Logic Programming (CLP) is an extension of Logic Programming aimed at replacing the pattern matching mechanism of unification, as used in Prolog, by a more general operation called constraint satisfaction. This aritcle provides a panoramic view of the recent work done in designing and implementing CLP languages. It also presents a summary of their theoretical foundations, discusses implementation issues, compares the major CLP languages, and suggests directions for further work.< ...

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Title
Computer **simulation** of **combinatorial** and sequential **logic** circuits.

Author(s)
Jorke-G.

Source
Nachrichtentechnik-Elektronik (East Germany), vol.23, no.9, p.322-3, 1973.

CODEN
NTELAP.

ISSN
ISSN: 0323-4657.

Publication year
1973.

Language
GE.

Publication type
J Journal Paper.

Treatment codes
P Practical.

Abstract
A general description is given of a Fortran program developed for static and dynamic **simulation** of **logic** circuits. Input and output structures are illustrated. Standard gates, flip-flops, adders, shift registers etc. are allowed, and no mention is made of the modelling problem. The limiting number of nodes is 500. (0 refs).

Descriptors
computer-aided-circuit-analysis; computer-aided-logic-design; logic-circuits; simulation.

Keywords
computer **simulation;** sequential **logic** circuits; general description; FORTRAN program; dynamic **simulation;** output structures; up to 500 modes; **combinatorial logic** circuits.

Classification codes

B1260 (Pulse circuits other than digital electronics).
B1265 (Digital electronics).
C5210B (Computer-aided **logic design**).

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☐	L2	simulat$ and (logic near/5 design) and (combinatorial logic or state logic) and (separate same graphical element?)	0
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L1: Entry 1 of 13 File: PGPB Jul 17, 2003

PGPUB-DOCUMENT-NUMBER: 20030135355
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20030135355 A1

TITLE: Modeling a logic design

PUBLICATION-DATE: July 17, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Wheeler, William R.	Southborough	MA	US	
Fennell, Timothy J.	Holliston	MA	US	

US-CL-CURRENT: 703/14

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw Desc | Image

☐ 2. Document ID: US 20030051223 A1

L1: Entry 2 of 13 File: PGPB Mar 13, 2003

PGPUB-DOCUMENT-NUMBER: 20030051223
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20030051223 A1

TITLE: Generating a logic design

PUBLICATION-DATE: March 13, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Wheeler, William R.	Southborough	MA	US	
Adiletta, Matthew J.	Worcester	MA	US	
Fennell, Timothy J.	Holliston	MA	US	

US-CL-CURRENT: 716/18

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw Desc | Image

3. Document ID: US 20030046649 A1

L1: Entry 3 of 13 File: PGPB Mar 6, 2003

PGPUB-DOCUMENT-NUMBER: 20030046649
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20030046649 A1

TITLE: Model-based logic design

PUBLICATION-DATE: March 6, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Wheeler, William R.	Southborough	MA	US	
Adiletta, Matthew J.	Worcester	MA	US	
Clark, Christopher	Hopkinton	MA	US	
Fennel, Timothy J.	Holliston	MA	US	

US-CL-CURRENT: 716/12

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw Desc | Image

4. Document ID: US 20030046648 A1

L1: Entry 4 of 13 File: PGPB Mar 6, 2003

PGPUB-DOCUMENT-NUMBER: 20030046648
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20030046648 A1

TITLE: Displaying information relating to a logic design

PUBLICATION-DATE: March 6, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Wheeler, William R.	Southborough	MA	US	
Adiletta, Matthew J.	Worcester	MA	US	

US-CL-CURRENT: 716/11

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw Desc | Image

5. Document ID: US 20030046642 A1

L1: Entry 5 of 13 File: PGPB Mar 6, 2003

PGPUB-DOCUMENT-NUMBER: 20030046642

PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20030046642 A1

TITLE: Employing intelligent logical models to enable concise logic representations for clarity of design description and for rapid design capture

PUBLICATION-DATE: March 6, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Wheeler, William R.	Southborough	MA	US	
Fennell, Timothy J.	Holliston	MA	US	
Adiletta, Matthew J.	Worcester	MA	US	

US-CL-CURRENT: 716/2

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw Desc | Image

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☐ 6. Document ID: US 20030046640 A1

L1: Entry 6 of 13 File: PGPB Mar 6, 2003

PGPUB-DOCUMENT-NUMBER: 20030046640
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20030046640 A1

TITLE: Generating a logic design

PUBLICATION-DATE: March 6, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Wheeler, William R.	Southborough	MA	US	
Adiletta, Matthew J.	Worcester	MA	US	

US-CL-CURRENT: 716/1

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw Desc | Image

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☐ 7. Document ID: US 20030046054 A1

L1: Entry 7 of 13 File: PGPB Mar 6, 2003

PGPUB-DOCUMENT-NUMBER: 20030046054
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20030046054 A1

TITLE: Providing modeling instrumentation with an application programming interface to a GUI application

PUBLICATION-DATE: March 6, 2003

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INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Wheeler, William R.	Southborough	MA	US	
Adiletta, Matthew J.	Worcester	MA	US	
Fennell, Timothy J.	Holliston	MA	US	

US-CL-CURRENT: 703/15

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw Desc | Image

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☐ 8. Document ID: US 20030046053 A1

L1: Entry 8 of 13 File: PGPB Mar 6, 2003

PGPUB-DOCUMENT-NUMBER: 20030046053
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20030046053 A1

TITLE: Logic simulation

PUBLICATION-DATE: March 6, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Wheeler, William R.	Southborough	MA	US	
Fennell, Timothy J.	Holliston	MA	US	
Adiletta, Matthew J.	Worcester	MA	US	

US-CL-CURRENT: 703/15

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw Desc | Image

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☐ 9. Document ID: US 20030046052 A1

L1: Entry 9 of 13 File: PGPB Mar 6, 2003

PGPUB-DOCUMENT-NUMBER: 20030046052
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20030046052 A1

TITLE: Simulating a logic design

PUBLICATION-DATE: March 6, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Wheeler, William R.	Southborough	MA	US	
Adiletta, Matthew J.	Worcester	MA	US	

US-CL-CURRENT: 703/15

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw Desc | Image

☐ 10. Document ID: US 20030046051 A1

L1: Entry 10 of 13 File: PGPB Mar 6, 2003

PGPUB-DOCUMENT-NUMBER: 20030046051
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20030046051 A1

TITLE: Unified design parameter dependency management method and apparatus

PUBLICATION-DATE: March 6, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Wheeler, William R.	Southborough	MA	US	
Adiletta, Matthew J.	Worcester	MA	US	
Fennell, Timothy J.	Holliston	MA	US	

US-CL-CURRENT: 703/14

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw Desc | Image

☐ 11. Document ID: US 6721925 B2

L1: Entry 11 of 13 File: USPT Apr 13, 2004

US-PAT-NO: 6721925
DOCUMENT-IDENTIFIER: US 6721925 B2

TITLE: Employing intelligent logical models to enable concise logic representations for clarity of design description and for rapid design capture

DATE-ISSUED: April 13, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Wheeler; William R.	Southborough	MA		
Fennell; Timothy J.	Holliston	MA		
Adiletta; Matthew J.	Worcester	MA		

US-CL-CURRENT: 716/2; 716/18, 716/3, 716/7

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

☐ 12. Document ID: US 6708321 B2

L1: Entry 12 of 13 File: USPT Mar 16, 2004

US-PAT-NO: 6708321
DOCUMENT-IDENTIFIER: US 6708321 B2
** See image for Certificate of Correction **

TITLE: Generating a function within a logic design using a dialog box

DATE-ISSUED: March 16, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Wheeler; William R.	Southborough	MA		
Adiletta; Mathew J.	Worcester	MA		
Fennell; Timothy J.	Holliston	MA		

US-CL-CURRENT: 716/18; 716/3

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWMC | Draw Desc | Image

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☐ 13. Document ID: US 6643836 B2

L1: Entry 13 of 13 File: USPT Nov 4, 2003

US-PAT-NO: 6643836
DOCUMENT-IDENTIFIER: US 6643836 B2

TITLE: Displaying information relating to a logic design

DATE-ISSUED: November 4, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Wheeler; William R.	Southborough	MA		
Adiletta; Matthew J.	Worcester	MA		

US-CL-CURRENT: 716/11; 703/16, 716/18, 716/3, 716/4

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWMC | Draw Desc | Image

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Term	Documents
WHEELER	17592
WHEELERS	446
LOGIC	391480
LOGICS	4259